YAMAHA LSI

YM3428

Surround Processor-B (SP-B)

■ Introduction

The YM3428, a 16-pin DIP C-MOS LSI, permits to implement quality digital surround sound capabilities realized by Yamaha's digital audio signal processing technology.

As the LSI includes A/D and D/A converters, you can easily implement digital surround functions as an analog input/output device.

As it has four delay lines each of which may be set for the maximum delay time of 30.24 msec, and outputs in two channels by adding delays of each of two pairs of delay lines, the range of application is wide.

■ Features

- Three kinds of surround mode are possible as preset modes without the use of any microcomputers.
- With a use of microprocessor, it is possible to set the four delay lines at different delay times and different volumes and to define parameters of a primary IIR digital low-pass filter for input.
- The internal signal format is of 14-bit floating point type processed digitally.
- The built-in A/D and D/A converters are of floating type with high linearity.
- The built-in reference voltage generator for A/D Converter permits an interface with analog circuits.
- The sampling frequency of A/D conversion is 24.9 kHz, so the bandwidth needed for surround sounds is secured.
- External low-pass filter is eliminated by employing the quadruple oversampling digital filter processing which uses 99.4 kHz D/A conversion sampling frequency.
- Distortion is as low as 0.22% (typical) at the maximum output of 1 kHz.

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YM3428 CATALOG
CATALOG No. : LSI-2134282
1992.02

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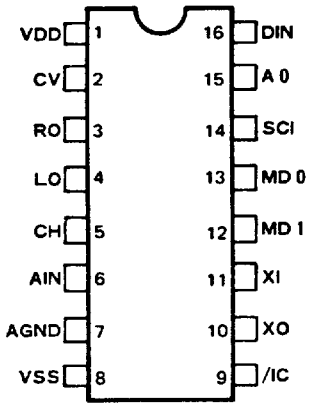
■ Package pin arrangement



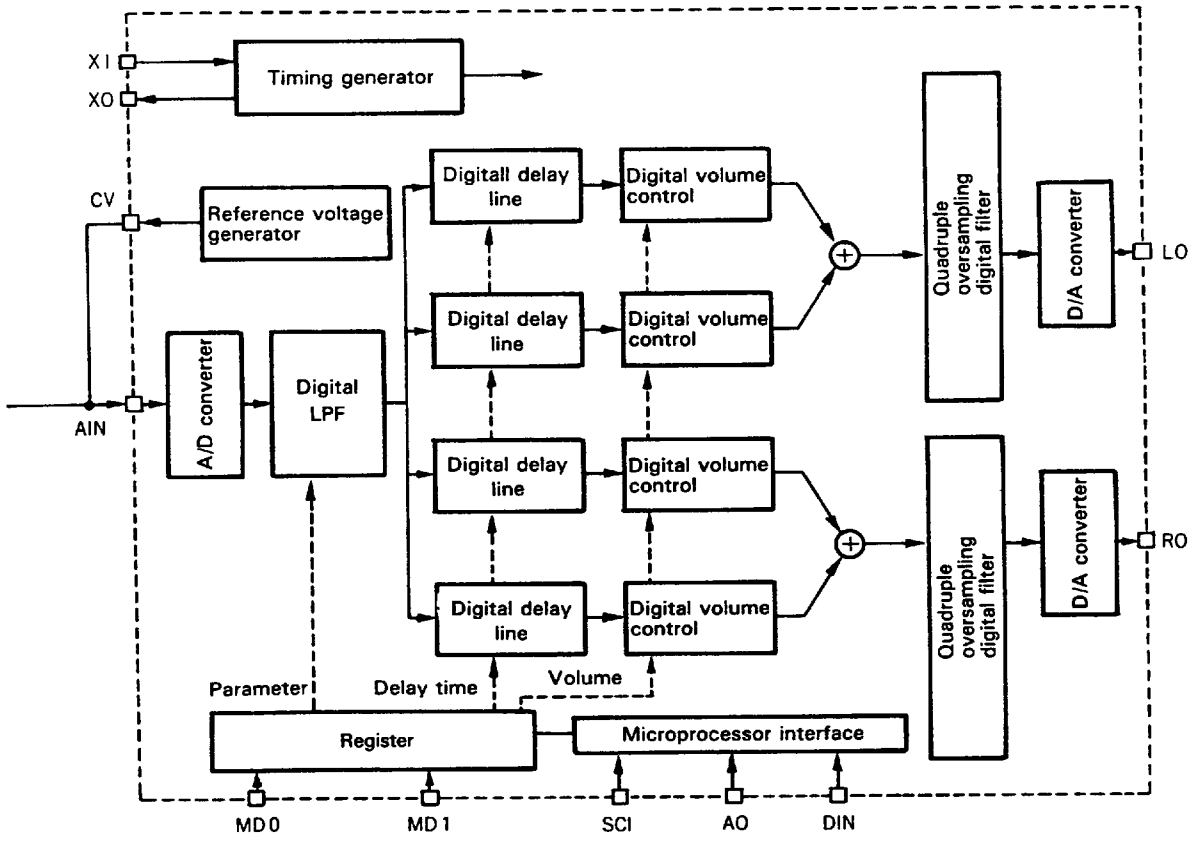
TOP VIEW

■ Pin assignments

Pin No.	Symbol	I/O	Description
1	VDD	—	+5V power
2	CV	O	+2.5V reference voltage (output) for A/D converter
3	RO	O	R-channel output (D/A conversion analog output)
4	LO	O	L-channel output (D/A conversion analog output)
5	CH	O	Connects to external sample-hold capacitor
6	AIN	I	Analog signal input (with CV as reference voltage)
7	AGND	—	Ground of A/D and D/A converters (must be connected to VSS externally)
8	VSS	—	System ground of digital circuits
9	/IC	*I	Reset terminal
10 11	XO XI	O I	Connects to a quartz crystal oscillator (Input of external clock signal, if used)
12 13	MD1 MD0	*I *I	Mode setting terminal
14 15 16	SCI A0 DIN	I I I	Clock input for data shift when a microprocessor is used Input of address/data identifying signal when a microprocessor is used Data input when a microprocessor is used

* indicates that a pullup resistor is built in.

■ Block diagram



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■ System block diagram

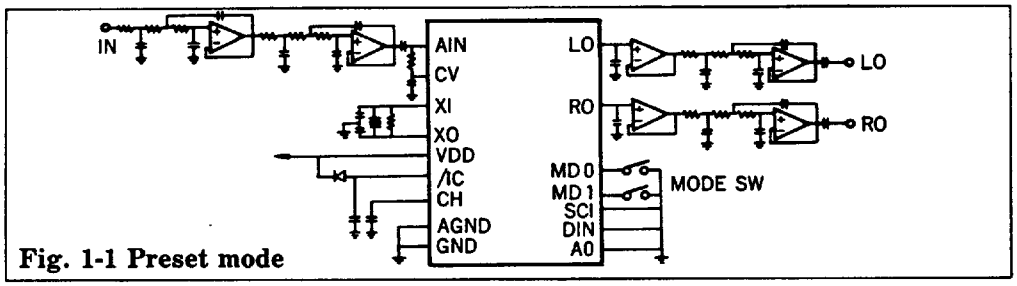

Fig. 1-1 Preset mode

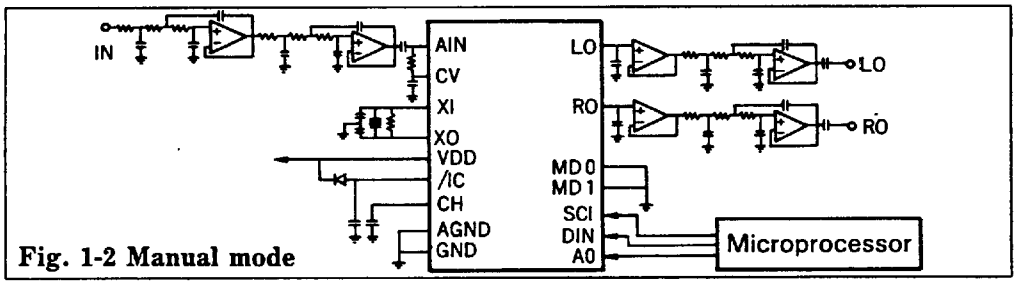

Fig. 1-2 Manual mode

■ Description

As shown in a block diagram below, analog input signal coming to the terminal AIN enters a 14-bit floating A/D converter, which samples the input signal at the rate of 24.9 kHz and converts it to digital signal format of 14-bit floating point numbers. The output of the A/D conveter enters a primary IIR LPF. (The cutoff frequency of this filter may be controlled with the parameters set in the registers A0, A1 and B1 from a microprocessor connected.)
The digital delay unit consisting of RAM has four output taps which can be switched by the parameters set in the registers DL0, DL1, DR0 and DR1.
The output signals come from the taps to digital volume units. In these units, volume registers GL0, GL1 and GR1 decay the signal levels digitally. Then adders produce L0+L1 and R0+R1. These outputs enter quadruple oversampling digital filters individually. This oversampling filter decays the input signal by about 25 dB in its cutoff region to reduce loop-back noises which would appear after D/A conversion. This eliminates the external LPF at the output circuit. The sampling rate of the digital input to the D/A converter is quadrupled, i.e., 99.4kHz.
To perform such digital processing, the LSI executes ROM programs.
In a preset mode, parameters will be provided as ROM data, so the microprocessor is not necessary to supply parameters.

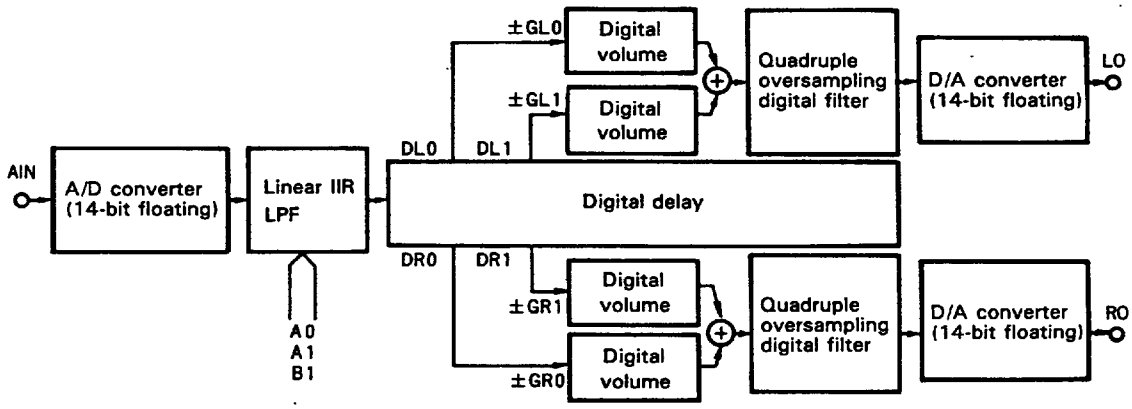

Fig. 2 Internal processing

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■ Setting preset modes and characteristics

- **[Hall Surround]** (MD0="L", MD1="H")
  Hall surround signals LO and RO is produced from level difference between long and intermediate delays. When the L+R signal (monaural) comes to the AIN terminal, Hall Surround effect will occur.
- **[Simulated Stereo]** (MD0="H", MD1="L")
  Simulated stereo signals LO and RO are produced from a monaural input signal by inverting phase of long delay with high level and short delay with low level, so that a comb filter with level difference is formed. The L+R signal input causes LO and RO to come out through the front speakers.
- **[Simple Delay]** (MD0="H", MD1="H")
  The signal output from LO is delayed by 20.16 ms and that from RO is delayed by 30.24 ms.

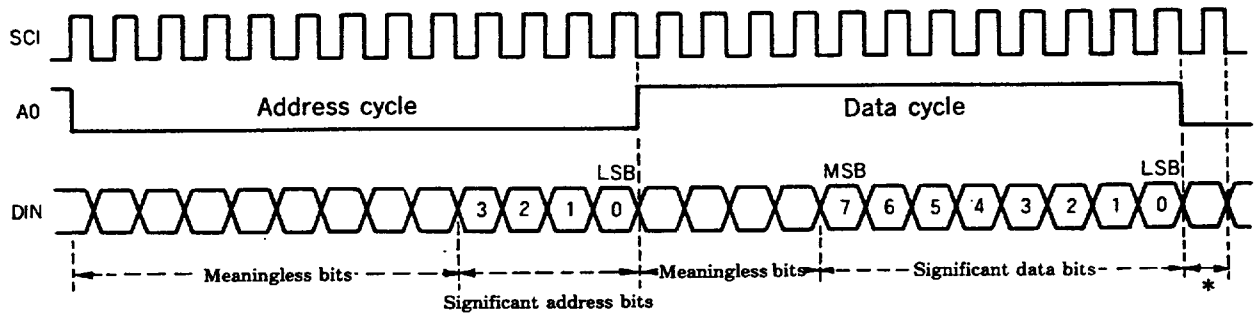
■ Register address map

The LSI operates in manual mode when MD0="L" and MD1="L". To use the LSI in manual mode, data must be set in the registers as listed below through a microprocessor.

Address (HEX)	Data/registers D7	D6	D5	D4	D3	D2	D1	D0	Parameter
00	X	X	±	DL 0					Lch 0 polarity/delay time
01	X	X	±	DL 1					Lch 1 polarity/delay time
02	X	X	±	DR 0					Rch 0 polarity/delay time
03	X	X	±	DR 1					Rch 1 polarity/delay time
04	GL 1							GL 0	L-channel volume level
05	GR 1							GR 0	R-channel volume level
06	X	X	X	X	A 0 (High order)				LPF parameter A 0
07	A 0 (Low order)								
08	X	X	X	X	A 1 (High order)				LPF parameter A 1
09	A 1 (Low order)								
0A	X	X	X	X	B 1 (High order)				LPF parameter B 1
0B	B 1 (Low order)								

Notes * : X means either "0" or "1".
* : Data may be written in the registers whatever values MD0 and MD1 are set at.
* : Mute the outputs while writing in LPF parameters : otherwise unusual sounds might be produced.

- **Microprocessor interface**



* After the fall of AO in the last data, send out SCI for one clock period or more.

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■ Register data

- **Setting output polarity ($0 ~ $3 D5 : ±)**
  When D5="1", the output signal is in phase with the input signal.
  When D5="0", the output signal is in opposite phase with the input signal.
- **Setting delay time ($0 ~ $3 : DL0, DL1, DR0, DR1)**

Delay time (mS)	D 4	D 3	D 2	D 1	D 0
0	0	0	0	0	0
1.44	0	0	0	0	1
2.88	0	0	0	1	0
4.32	0	0	0	1	1
5.76	0	0	1	0	0
7.20	0	0	1	0	1
8.64	0	0	1	1	0
10.08	0	0	1	1	1
11.52	0	1	0	0	0
12.96	0	1	0	0	1
14.40	0	1	0	1	0

Delay time (mS)	D 4	D 3	D 2	D 1	D 0
15.84	0	1	0	1	1
17.68	0	1	1	0	0
18.72	0	1	1	0	1
20.16	0	1	1	1	0
21.60	0	1	1	1	1
23.04	1	0	0	0	0
24.48	1	0	0	0	1
25.92	1	0	0	1	0
27.36	1	0	0	1	1
28.80	1	0	1	0	0
30.24	1	0	1	0	1

Note : Input beyond "10101" is prohibited, (unusual sound would be produced.)

- **Setting volume level ($4, $5 : GL0, GL1, GR0, GR1)**

Volume level		D 3	D 2	D 1	D 0	GL 0, GR 0
(Decimal)	(dB)	D 7	D 6	D 5	D 4	GL 1, GR 1
0.875	−1.16	1	1	1	1	
0.74	−2.50	1	1	1	0	
0.625	−4.08	1	1	0	1	
0.5	−6.00	1	1	0	0	
0.4375	−7.18	1	0	1	1	
0.375	−8.52	1	0	1	0	
0.3125	−10.1	1	0	0	1	
0.25	−12.0	1	0	0	0	
0.21875	−13.2	0	1	1	1	
0.1875	−14.5	0	1	1	0	
0.15625	−16.1	0	1	0	1	
0.125	−18.1	0	1	0	0	
0.109375	−19.2	0	0	1	1	
0.09375	−20.6	0	0	1	0	
0.078125	−22.1	0	0	0	1	
0		0	0	0	0	

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- **Setting LPF parameters ($6~$B : A0, A1, B1)**

Register	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
A0	Address $6								Address $7							
A1	Address $8								Address $9							
B1	Address $A								Address $B							
bit	X	X	X	X	11	10	09	08	07	06	05	04	03	02	01	00
Parameter					SIN	Exponent			Mantissa							

△ Decimal point position

SIN is a sign bit; "1" for plus and "0" for minus.
The exponent means that, when its value is EX, the parameter value is given by the mantissa multiplied by the EXth power of 2.

bit D10	D9	D8	D7	EX	(decimal)
0	0	0	0	−0	1
1	1	1	1	−1	0. 5
1	1	1	0	−2	0. 2 5
1	1	0	1	−3	0. 1 2 5
1	1	0	0	−4	0. 0 6 2 5
1	0	1	1	−5	0. 0 3 1 2 5
1	0	1	0	−6	0. 0 1 5 6 2 5
1	0	0	1	−7	0. 0 0 7 8 1 2 5
1	0	0	0	−8	0. 0 0 3 9 0 6 2 5

The mantissa is bits 6—0 with the decimal point existing between bit 6 and 5. The mantissa must be normalized in such a manner that the content of bit 6 is 1, unless the value is 0.

[Examples of parameters]

f c	$6	$7	$8	$9	$A	$B
3 KHz	00001111	01001001	00001111	01001001	00001111	01101110
4 KHz	00001111	01011011	00001111	01011011	00001111	01001010
5 KHz	00001111	01101100	00001111	01101100	00001110	11010000
6 KHz	00001111	01111100	00001111	01111100	00001101	11000000
7 KHz	00001111	11000110	00001111	11000110	00000110	01100000
8 KHz	00001111	11001110	00001111	11001110	00000110	11110000
Flat	00001000	01000000	00000000	00000000	00000000	00000000

■ Electrical characteristics

- **1. Absolute maximum ratings (V_{SS}=0.0V)**

Item	Symbol	Rating	Unit
Terminal voltage	V_{DD}—V_{SS}	−0.3~7.0	V
Operating temperature	T_{OP}	0~70	°C
Storage temperature	T_{STG}	−50~125	°C

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- 2. Recommended operating conditions (V_{SS}=0.0V, T_{OP}=0~70 °C)

Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	4.75	5.00	5.25	V
	V_{SS}, AGND	0	0	0	V

- 3. DC characteristics (V_{DD}=4.75~5.25V, T_{OP}=0~70 °C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Low-level input voltage	V_{IL}		−0.3		0.8	V
High-level input voltage	V_{IH}	Except XI	2.0		V_{DD}	V
High-level input voltage	V_{IH}	XI	4.0		V_{DD}	V
Low-level output voltage	V_{OL}	XO : I_{OL}=0.2 mA	−0.3		0.4	V
High-level output voltage	V_{OH}	XO : I_{OH}=0.4 mA	4.0			V
Input current leak	I_{LK}	VI=5V			10	μA
Supply current	I_{DD}			20.0	30.0	mA
Input capacitance	C_I	f=1 MHz			10	pF
Output capacitance	C_O				10	pF
Pullup resistance	R_{PU}	/IC, MD0, MD1	50		400	KΩ

- 4. AC characteristics (V_{DD}=4.75~5.25V, T_{OP}=0~70 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
XI clock input frequency	fc	1.8	3.58	4.5	MHz
XI clock input duty		40	50	60	%
XI clock rise time				50	ns
XI clock fall time				50	ns
SCI clock input frequency				fc × 1/4	MHz
SCI clock on time		600			ns
SCI clock rise time				200	ns
SCI clock fall time				200	ns

- 5. Analog characteristics (V_{DD}=5.0V, T_{OP}=0~70 °C)

Parameter	Symbol	Condition	TYP.	MAX.	Unit
Analog input voltage	V_{IA}	AIN		4.2	VP−P
Analog output voltage (*1)	V_{OA}	RO, LO		V_{DD}	VP−P
DC offset voltage	C_V		2.5		V
Total harmonic distortion (*2)	THD	1 kHz			
		0 dB	0.22	0.27	%
		−10 dB	0.25	0.30	%
		−20 dB	0.35	0.45	%
		−30 dB	0.7	1.2	%
Signal-to-noise ratio (*3)	S/N		80		dB

Notes *1 : External resistance RL=5 MΩ
*2 : The total harmonic distortion here is THD+noise.
fc=3.58 MHz, input signal frequency=1 kHz, internal LPF=flat (through), with external filter (cutoff frequency 10 kHz, 18 db/oct) at output
*3 : fc=3.58 MHz, internal LPF=flat (through),
Output side external filter (cutoff frequency 10 kHz, 18 db/oct) is used at 4.2 Vp-p input for S and at no signal input for N.

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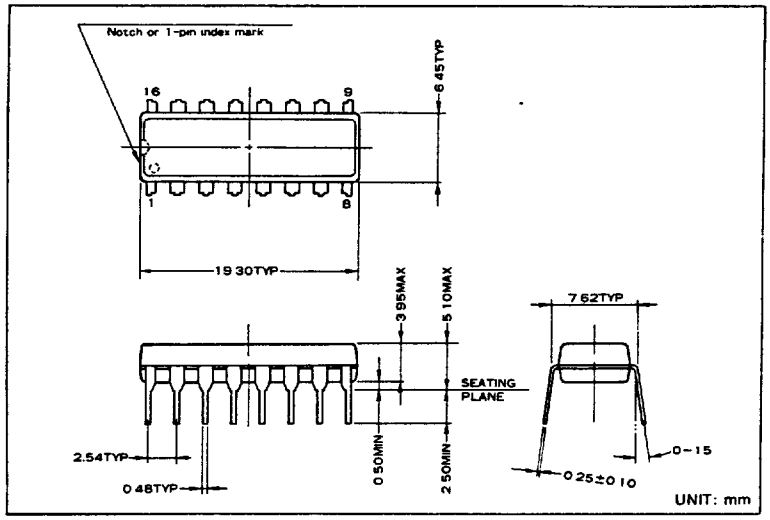
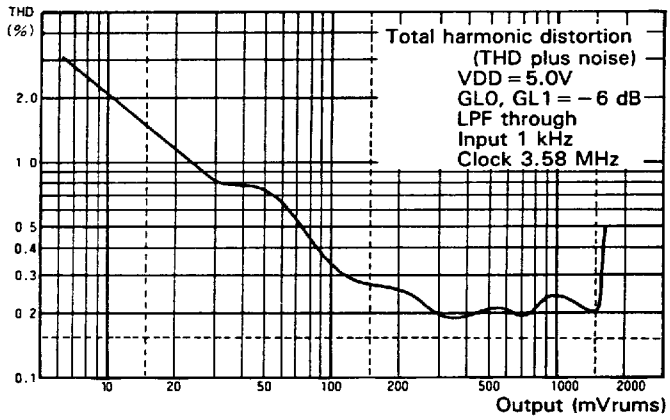
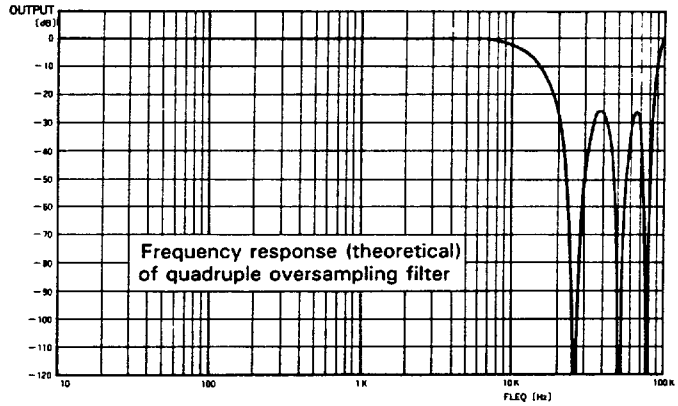
■ External views



■ Characteristics (reference data)





Notes :
- The YM3428 and YM3411 are almost the same. The only differences are in the sampling frequency of the built-in A/D converter, whether or not an undersampling filter is incorporated, and in THD.
  Compared with the YM3411, the YM3428 requires the cutoff characteristic of the external LPF at the input to be more steep. But THD will be so much the better.
- The specifications are subject to changes for improvement without prior notice.
- The standard clock frequency of XI is 3.58 MHz in this catalog.

AGENCY

YAMAHA CORPORATION

Address inquiries to:
Semi-conductor Sales Department
■ Head Office 203, Matsunokijima, Toyooka-mura, Iwata-gun, Shizuoka-ken, 438-01
Electronic Equipment business section
Tel. 0539-62-4918 Fax. 0539-62-5054
■ Tokyo Office 2-17-11, Takanawa, Minato-ku, Tokyo, 108
Tel. 03-5488-5431 Fax. 03-5488-5088
■ Osaka Office 3-12-9, Minami Senba, Chuo-ku, Osaka City, Osaka, 542
Shinsaibashi Plaza Bldg. 4F
Tel. 06-252-7980 Fax. 06-252-5615
■ U.S.A. Office YAMAHA Systems Technology.
100 Century Center Court, San Jose, CA95112
Tel. 408-467-2300 Fax. 408-437-8791

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